Serial Number: 10/790,510 Filing Date: March 1, 2004

Title: STATIC PASS TRANSISTOR LOGIC WITH TRANSISTORS WITH MULTIPLE VERTICAL GATES

Conclusion

The specification has been amended to update the priority information. Claim 41 has been amended to correct a typographical error.

It is respectfully submitted that these changes do not introduce new matter, and the claims are allowable without further search or consideration. Therefore, entry is appropriate under Rule 312, and is respectfully requested.

Respectfully submitted,

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<u>CERTIFICATE UNDER 37 CFR 1.8:</u> The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop Issue Fee, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this One of November, 2005.

Eric H. Okon

Signature